

FIG.1
RELATED ART

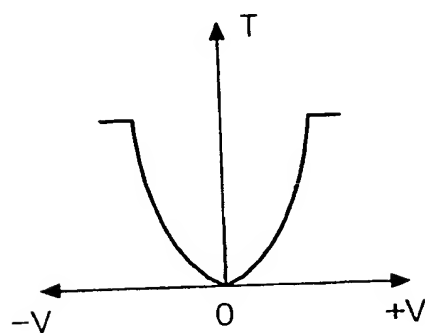


FIG.2
RELATED ART

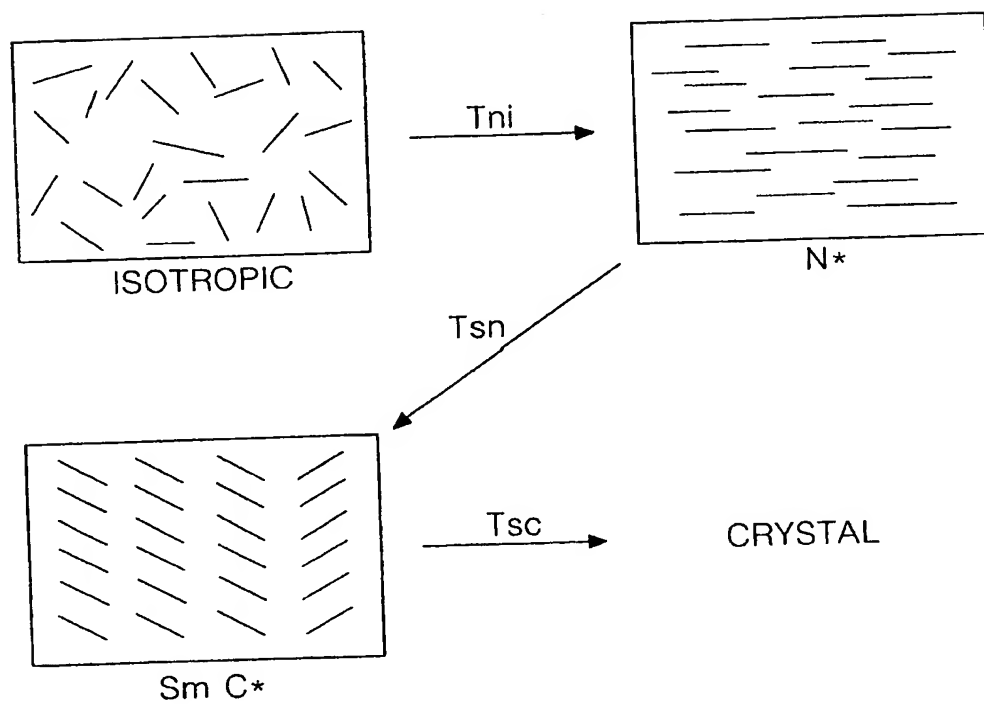
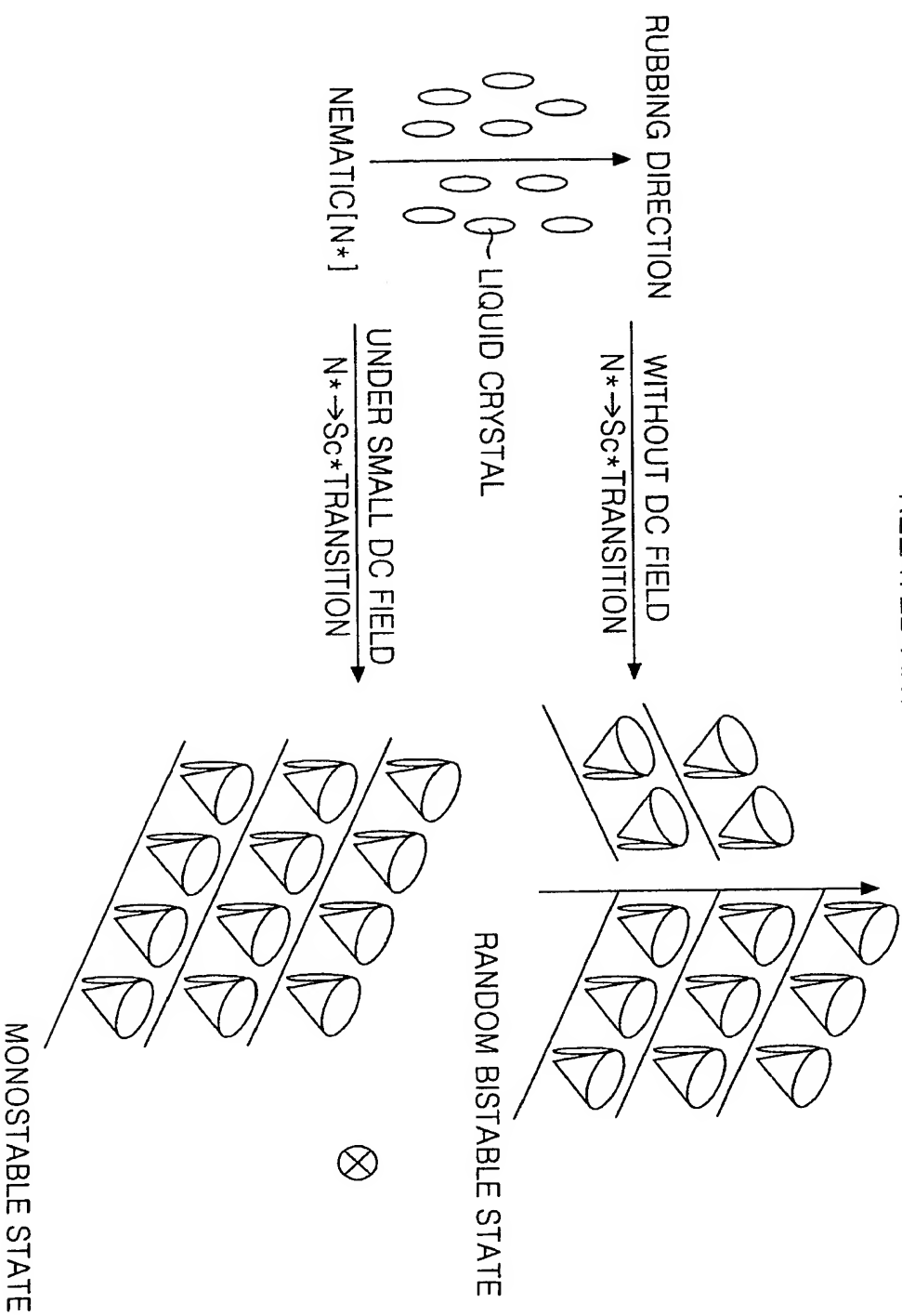


FIG. 3
RELATED ART



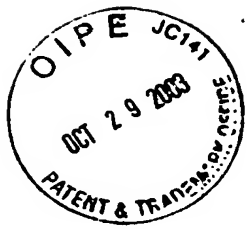


FIG.4A
RELATED ART

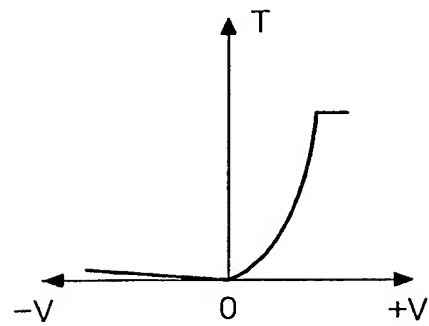


FIG.4B
RELATED ART

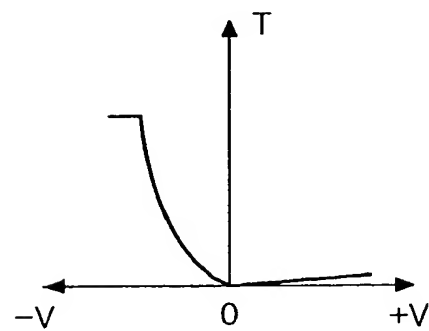




FIG.5A
RELATED ART

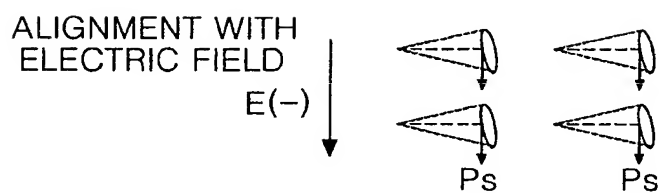
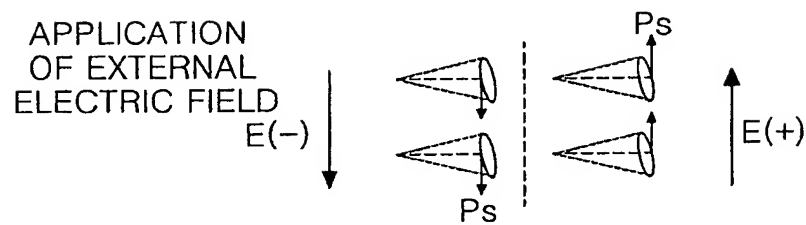


FIG.5B
RELATED ART



The diagram illustrates a pixel circuit architecture. It features a horizontal row of transistors labeled 60, 61, and 64. A vertical column of transistors is shown on the left, with labels 67 and 66. The circuit includes various input signals: VH , VL , $Vcom$, GND , and Vcc . Specific nodes are identified as 65a, 65b, 68a, and 68b. The output signal is labeled 62. The circuit also includes a series of gates or switches labeled $DL1$, $DL2$, ..., $DLm-1$, DLm . Other components include Cic , Cst , TFT , and I .



FIG.7

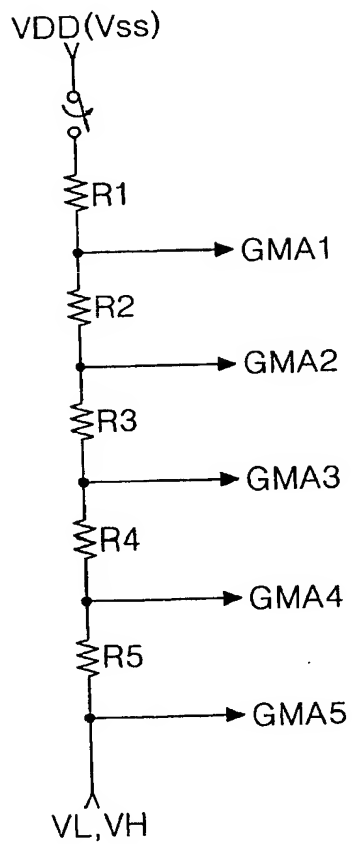


FIG.8

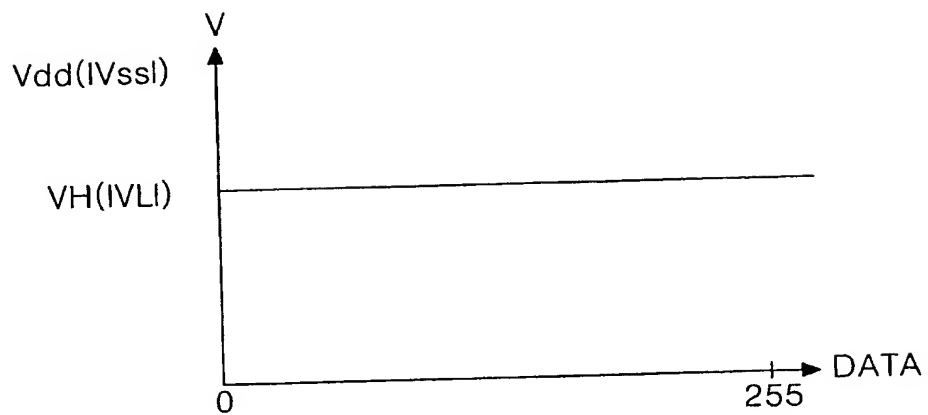




FIG.9

